THAT WHICH IS CLAIMED IS:

1. An integrated circuit device comprising:

an integrated circuit substrate having a cell array region and a peripheral circuit region;

a buried contact plug on the integrated circuit substrate in the cell array region;

a resistor on the integrated circuit substrate in the peripheral circuit region;

a first pad contact plug on the buried contact plug;

a second pad contact plug on the resistor; and

an ohmic layer between the first pad contact plug and the buried contact plug and between the second pad contact plug and the resistor.

2. The integrated circuit device of Claim 1, further comprising:

a lower interlayer dielectric layer on the integrated circuit substrate, wherein the lower interlayer dielectric layer defines a contact hole in the cell array region, wherein the buried contact plug is disposed in the contact hole and wherein the resistor is disposed on the lower interlayer dielectric layer; and

a first interlayer dielectric layer on the lower interlayer dielectric layer, the buried contact plug and the resistor, wherein the first interlayer dielectric layer defines a first pad contact hole in the cell array region and a second pad contact hole in the peripheral circuit region and wherein the first and second pad contact plugs are disposed in the first and second pad contact holes, respectively.

3. The integrated circuit device of Claim 2, further comprising:

a capacitor including a lower electrode on the first pad contact plug, a capacitor dielectric layer on the lower electrode, and an upper electrode on the capacitor dielectric layer;

a second interlayer dielectric layer on the capacitor and the first interlayer dielectric layer, the second interlayer dielectric layer defining a metal contact hole in the peripheral circuit region; and

a metal contact plug in the metal contact hole in the peripheral circuit region.

4. The integrated circuit device of Claim 3, further comprising an etch stop layer between the first interlayer dielectric layer and the second interlayer dielectric layer.

5. The integrated circuit device of Claim 1, wherein the ohmic layer comprises at least one of titanium silicide (TiSi), tantalum silicide (TaSi), cobalt silicide

(CoSi) and nickel silicide (NiSi).

6. The integrated circuit device of Claim 3, further comprising:

a first adhesion layer between the first pad contact plug and the first interlayer dielectric layer, between the first pad contact plug and the buried contact plug, between the second pad contact plug and the first interlayer dielectric layer, and between the second pad contact plug and the resistor; and

a second adhesion layer between the metal contact plug and the second interlayer dielectric layer and between the metal contact plug and the second pad contact plug.

7. The integrated circuit device of Claim 3, wherein the first pad contact plug, the second pad contact plug and the metal contact plug comprise at least one of tungsten, aluminum, copper, doped polysilicon and undoped polysilicon.

8. The integrated circuit device of Claim 1, wherein the buried contact plug and the resistor comprise the same material.

9. A method of forming an integrated circuit device comprising:

forming a buried contact plug on a cell array region of an integrated circuit substrate;

forming a resistor on a peripheral circuit region of the integrated circuit substrate;

forming a first pad contact plug on the buried contact plug;

forming a second pad contact plug on the resistor; and

forming an ohmic layer between the first pad contact plug and the buried contact plug and between the second pad contact plug and the resistor.

10. The method of Claim 9, wherein forming the ohmic layer is followed by:

forming a capacitor including a lower electrode on the first pad contact plug, a capacitor dielectric layer on the lower electrode, and an upper electrode on the capacitor dielectric layer.

11. The method of Claim 10, wherein forming the capacitor is preceded by:

forming a lower interlayer dielectric layer on the integrated circuit substrate, wherein the lower interlayer dielectric layer defines a contact hole in the cell array region, wherein the buried contact plug is disposed in the contact hole and wherein the resistor is disposed on the lower interlayer dielectric layer; and

forming a first interlayer dielectric layer on the lower interlayer dielectric layer, the buried contact plug and the resistor, wherein the first interlayer dielectric layer defines a first pad contact hole in the cell array region and a second pad contact hole in the peripheral circuit region and wherein the first and second pad contact plugs are disposed in the first and second pad contact holes, respectively.

12. The method of Claim 11, further comprising:

forming a second interlayer dielectric layer on the capacitor and the first interlayer dielectric layer, the second interlayer dielectric layer defining a metal contact hole in the peripheral circuit region; and

forming a metal contact plug in the metal contact hole in the peripheral circuit region.

13. The method of Claim 12, further comprising forming an etch stop layer between the first interlayer dielectric layer and the second interlayer dielectric layer.

14. The method of Claim 12, further comprising:

forming a first adhesion layer between the first pad contact plug and the first interlayer dielectric layer, between the first pad contact plug and the buried contact plug, between the second pad contact plug and the first interlayer dielectric layer, and between the second pad contact plug and the resistor; and

forming a second adhesion layer between the metal contact plug and the second interlayer dielectric layer and between the metal contact plug and the second pad contact plug.

15. A method of forming an integrated circuit device comprising:

forming an ohmic layer between a first pad contact plug and a buried contact plug in a cell array region of an integrated circuit substrate and between a second pad contact plug and a resistor in a peripheral circuit region of the integrated circuit substrate; and then

forming a capacitor on the first pad contact plug in the cell array region of the integrated circuit substrate.

16. The method of Claim 15, wherein forming the capacitor comprises:

forming a lower electrode on the first pad contact plug;

forming a capacitor dielectric layer on the lower electrode; and

forming an upper electrode on the capacitor dielectric layer.

17. The method of Claim 15, wherein forming the capacitor is preceded by:

forming the buried contact plug on the cell array region of the integrated circuit substrate;

forming the resistor on the peripheral circuit region of the integrated circuit substrate;

forming the first pad contact plug on the buried contact plug in the cell array region; and

forming the second pad contact plug on the resistor in the peripheral circuit region.

18. The method of Claim 17, wherein forming the capacitor is further preceded by:

forming a lower interlayer dielectric layer on the integrated circuit substrate, wherein the lower interlayer dielectric layer defines a contact hole in the cell array region, wherein the buried contact plug is disposed in the contact hole and wherein the resistor is disposed on the lower interlayer dielectric layer; and

forming a first interlayer dielectric layer on the lower interlayer dielectric layer, the buried contact plug and the resistor, wherein the first interlayer dielectric layer defines a first pad contact hole in the cell array region and a second pad contact hole in the peripheral circuit region and wherein the first and second pad contact plugs are disposed in the first and second pad contact holes, respectively.

19. The method of Claim 18, further comprising:

forming a second interlayer dielectric layer on the capacitor and the first interlayer dielectric layer, the second interlayer dielectric layer defining a metal contact hole in the peripheral circuit region; and

forming a metal contact plug in the metal contact hole in the peripheral circuit region.

20. The method of Claim 19, further comprising forming an etch stop layer between the first interlayer dielectric layer and the second interlayer dielectric layer.

21. A method of forming an integrated circuit device comprising:

forming a lower interlayer dielectric layer on the integrated circuit substrate, the lower interlayer dielectric layer defining a contact hole exposing the integrated circuit substrate in a cell array region of the integrated circuit;

forming a first conductive layer in the contact hole and on the surface of the integrated

circuit substrate;

patterning the first conductive layer to provide a buried contact plug in the contact hole in the cell array region and a resistor on the lower interlayer dielectric layer in a peripheral circuit region of the integrated circuit substrate;

forming a first interlayer dielectric layer on the buried contact plug and the resistor;

patterning the first interlayer dielectric layer to provide a first pad contact hole exposing the buried contact plug and a second pad contact hole exposing at least a portion of the resistor; and

forming an ohmic layer on floors of the first and second pad contact holes.

22. A method of Claim 21, further comprising:

forming a second conductive layer on the ohmic layer and in the first and second pad contact holes;

planarizing the second conductive layer to expose the first interlayer dielectric layer and to provide a first pad contact plug in the first pad contact hole and a second pad contact plug in the second pad contact hole;

forming an etch stop layer on the first pad contact plug, the second pad contact plug and the first interlayer dielectric layer;

forming a capacitor including an upper electrode, a capacitor dielectric layer and a lower electrode on the first pad contact plug;

forming a second interlayer dielectric layer on a surface of the integrated circuit substrate;

patterning the second interlayer dielectric layer to provide a metal contact hole exposing the second pad contact plug in the peripheral circuit region; and

forming a third conductive layer in the metal contact hole to provide a metal contact plug.

23. The method of Claim 22, further comprising forming an etch stop layer on the integrated circuit substrate before forming the second interlayer dielectric layer.

24. The method of Claim 22, wherein forming an ohmic layer comprises:

forming a metal layer on the floors of the first pad contact hole and the second pad contact hole;

thermally treating the metal layer to form the ohmic layer between the metal layer and the buried contact plug and between the metal layer and the resistor.

25. The method of Claim 24, wherein the thermal treatment is performed at a temperature of about from about 600 to about 900 degrees Celsius for from about 10 to about 30 seconds.

26. The method of Claim 22,wherein forming the second conductive layer is preceded by forming a first adhesion layer in the first pad contact hole and the second pad contact hole; and

wherein forming the third conductive layer is preceded by forming a second adhesion layer in the metal contact hole.

27. The method of Claim 22, wherein forming a capacitor comprises:

forming a mold layer on the etch stop layer;

patterning the mold layer and the etch stop layer in the cell array region to form a storage node hole exposing the first pad contact plug;

forming a lower electrode layer on a surface of the integrated circuit substrate having the storage node hole;

forming a sacrificial layer in the storage node hole;

removing the lower electrode layer and the sacrificial layer on the mold layer by a planarization process to provide a lower electrode and a sacrificial pattern in the storage node hole;

removing the sacrificial pattern and the mold layer;

forming a dielectric layer and an upper electrode layer on the integrated circuit substrate having the lower electrode; and

removing at least the upper electrode layer in the peripheral circuit region of the integrated circuit substrate.

28. An integrated circuit device comprising:

an integrated circuit substrate having a cell array region and a peripheral circuit region;

a buried contact plug on the integrated circuit substrate in the cell array region;

a resistor on the integrated circuit substrate in the peripheral circuit region;

a first pad contact plug on the buried contact plug;

a second pad contact plug on the resistor; and

a silicide layer between the first pad contact plug and the buried contact plug and between the second pad contact plug and the resistor.

29. The integrated circuit device of Claim 28, further comprising:

a lower interlayer dielectric layer on the integrated circuit substrate, wherein the lower interlayer dielectric layer defines a contact hole in the cell array region, wherein the buried contact plug is disposed in the contact hole and wherein the resistor is disposed on the lower interlayer dielectric layer; and

a first interlayer dielectric layer on the lower interlayer dielectric layer, the buried contact plug and the resistor, wherein the first interlayer dielectric layer defines a first pad contact hole in the cell array region and a second pad contact hole in the peripheral circuit region and wherein the first and second pad contact plugs are disposed in the first and second pad contact holes, respectively.

30. The integrated circuit device of Claim 29, further comprising:

a capacitor including a lower electrode on the first pad contact plug, a capacitor dielectric layer on the lower electrode, and an upper electrode on the capacitor dielectric layer;

a second interlayer dielectric layer on the capacitor and the first interlayer dielectric layer, the second interlayer dielectric layer defining a metal contact hole in the peripheral circuit region; and

a metal contact plug in the metal contact hole in the peripheral circuit region.

31. The integrated circuit device of Claim 28, wherein the silicide layer comprises at least one of titanium silicide (TiSi), tantalum silicide (TaSi), cobalt silicide (CoSi) and nickel silicide (NiSi).

32. The integrated circuit device of Claim 30 further comprising:

a first adhesion layer between the first pad contact plug and the first interlayer dielectric layer, between the first pad contact plug and the buried contact plug, between the second pad contact plug and the first interlayer dielectric layer, and between the second pad contact plug and the resistor; and

a second adhesion layer between the metal contact plug and the second interlayer dielectric layer and between the metal contact plug and the second pad contact plug.

33. The integrated circuit device of Claim 28, wherein the buried contact plug and the resistor comprise the same material.